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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/492,243	01/27/2000	Yuesong He	M-7469-US	9620

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EXAMINER
ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/492,243	He Et.al.
Examiner	**Art Unit**
Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 7, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *3, 4, 9, and 12-14* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *3, 4, 9, and 12-14* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to a request for continued prosecution filed April 7, 2003 and on which Applicant amended claims 3, 4, 9 and 12.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 9, 12, 13 and 14 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Pio et.al. (U.S. Patent No. 5,894,146) in view of Davies et.al.(U.S. Patent No. 5,712,501). With regard to Claim 3, Pio teaches a memory array comprising a plurality of floating gate transistors (2) connected in series, each floating gate transistor having formed, in a well of a substrate, a source (15) region and a drain (16) region and a channel region separating said source and drain regions.

However, Pio fails to show a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant. Davies teaches a field effect transistor that includes a gate transistor having source and drain regions (13, 14) and channel region (16) separating the said source and drain regions, a dopant

concentration region (18) displaced about a target region, the target region situated below the channel region, and said dopant concentration region extending into the channel region, the channel region having a non-uniform concentration of dopant. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Pio to include a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant, as clearly suggested by Davies, in order to improve threshold voltage sensitivity in the channel region and drive capability and enhances punch-through resistance.

With regard to Claims 4 and 12, the claims contain the limitation "*said dopant concentration region is formed by a tilted ion implantation utilizing as a mask, at least a part of a gate structure of each floating gate transistor*", this is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by

process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

With regard to Claim 9, Pio teaches a memory array comprising a plurality of floating gate transistors (2) connected in series, each floating gate transistor having formed, in a well of a substrate, a source (15) region and a drain (16) region and a channel region separating said source and drain regions.

However, Pio fails to show a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant. Davies teaches a field effect transistor that includes a gate transistor having source and drain regions (13, 14) and channel region (16) separating the said source and drain regions, a dopant concentration region (18) displaced about a target region, the target region situated below the channel region, and said dopant concentration region extending into the channel region, the channel region having a non-uniform concentration of dopant. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Pio to include a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform

concentration of dopant, as clearly suggested by Davies, in order to improve both threshold voltage sensitivity in the channel region and drive capability and to enhance punch-through resistance.

With regard to Claims 13 and 14, Applicant merely labels the claimed invention as *"the transistor is an NMOS transistor"* and *"the NMOS transistor is a floating gate transistor"*, however, the claimed invention does not structurally distinguish from that taught by the prior art.

Response to Arguments

2. Applicant's arguments with respect to claims 3, 4, 9 and 12-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

4/16/03

SHEILA V. CLARK
PRIMARY EXAMINER